NEW Product

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UFE Series Front End Power Supplies

I²C Serial Bus Interface Application Note 210

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1. Introduction

This application note describes the I²C serial bus interface of the Artesyn Technologies' UFE series of Front End power supplies. The UFE series is designed to draw wide range input power and provide flexible (variable), isolated, floating, power-limited output in two configurations, 24 V and 48 V. Each configuration also provides an auxiliary output of 11 V at 250 mA. The UFE series also includes automatic-regulating fans for self-cooling. Automatic regulation of the cooling fans means getting the quietest possible operation while at the same time maximizing fan life. In addition to power conversion, the UFE series provides an enhanced set of features via I²C serial communication.

While the use of I²C serial communication is not required for operation, I²C serial communication is a very powerful tool that can greatly enhance and completes the feature set of the UFE series. Via I²C serial communication it is possible to adjust the output voltage (while power conversion is active), monitor a number of key input, output, and internal parameters, store and retrieve up to 175 bytes of EEPROM data, and enable/disable the power conversion process.

2. Functional Description

Within 2-seconds of initial power up the I²C interface can be used to monitor 4 analog parameters, 15 possible fault conditions, output power capability, general power conversion parameters, hours of operation, 64 bytes of ASCII encoded general manufacturing information, and 175 bytes of user selected information. The I²C interface can also be used at this time to change the output voltage of the converter, change the general power conversion parameters, and store up to 175 bytes of information in non-volatile memory. It is also possible to enable or disable the I²C interface by use of a discrete signal pin by the name of "I²C-En".

By default, this discrete signal pin is pulled high internally, which automatically enables the I²C interface. However, for troubleshooting purposes, when the "I²C-En" signal pin is pulled low, the I²C interface is physically isolated from the rest of the I²C bus. Pulling this discrete signal pin low will also reset the I²C hardware internally in the power supply, which can be quite valuable in resolving frozen I²C interface issues. A fully functional I²C interface consists of two basic types of commands, writes and reads.

Certain I²C write commands can be used with the general call address, 00h, or device specific commands. There are four basic write command types that can be used. The first write command is the All V-adjust command.

The All V-adjust command uses the general call address of 00h to change the output voltage of all UFE products connected to the I²C bus at the same time. This can be required if multiple UFE products are sharing the burden of sourcing power to a load. The voltage adjustment is determined by a 10-bit control code that is determined with the following equation:

$$48\text{ V unit: } Vout = 41.55 + (V_{adjcc}/1023) * 15.9$$

$$24\text{ V unit: } Vout = 20.78 + (V_{adjcc}/1023) * 7.95$$

Where Vadjcc is a decimal representation of the 10-bit output voltage adjustment control code, from 28 to 995. Vout represents the desired output voltage. This allows for voltage adjustments from 42 to 57 volts (+/- 1%), in approximately 15.5mV steps for the 48V unit, and from 21 to 28.5 volts (+/- 1%), in approximately 7.8mV steps for the 24V unit. Please note that if the output voltage droop function of the UFE is enabled (output voltage droop is default enabled for the 48 V unit and default disabled for the 24 V unit), the result of the voltage adjustment will vary with load. In order to produce a desired output voltage at any load, the output voltage droop function must be disabled and the active current sharing function enabled. It should also be noted that with the output voltage droop function enabled, adjustment limits are imposed to ensure that the output voltage will not be adjustable outside of the 42V to 57V or 21V to 28.5V range under any load conditions.

In order to prevent an accidental output voltage adjustment of the UFE power bus over I²C, an activation key must be used to unlock the All V-adjust feature. In order to adjust the voltage to all units, the correct activation key byte of 0xCD must be sent in the preceding byte. If the key is not correct, the output voltage will not change. The activation key must be sent each time the All V-adjust command is used.

The All V-adjust Command is constructed of three bytes, detailed in Table 1.

BYTE	4 (MSB)								3 ACTIVATION KEY BYTE								2								1 (LSB)							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Content	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	1	X	X	X	X	X	X	V_{adjcc} (0-1023)									

X - Denotes Not Used or Don't Caare Bit

Table 1 - All V-Adjust Command Structure

The second write command is the Individual V-adjust Command (command #1). As the name implies, this command will result in the output voltage changing on a single UFE output. The same formula as the All V-adjust Command should be used to determine the control code value, V_{adjcc}, required to get the desired output voltage, Vout:

48 V unit: $V_{adjcc} = ((Vout – 41.55)*1023)/15.9$

24 V unit: $Vout = 20.78 + (V_{adjcc}/1023) * 7.95$

The Individual V-adjust Command is constructed of four bytes, detailed in Table 2. The use of a command number byte allows shorter messages to be sent from the master to slave most of the time, which in turn helps to free up the I²C bus.

	I²C ADDRESS BYTE								COMMAND # BYTE								10-BIT V_{ADJCC}													
BYTE	4 (MSB)								3								2								1 (LSB)							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Content	UFE Address							0	0	0	0	0	0	0	0	1	X	X	X	X	X	X			V_{adjcc} (0-1023)							

X - Denotes Not Used or Don't Caare Bit

Table 2 - individual V-Adjust Command Structure

The third write command is the Individual Offset and Control Command (command #2). Each 48V UFE is calibrated via I²C at the factory to put out a regulated 52V +/- 1% with output voltage droop disabled and active current sharing enabled, measured at the output pins. Each 24V UFE is calibrated via I²C at the factory to put out a regulated 27V +/- 1% with output voltage droop disabled and active current sharing enabled, measured at the output pins. However, due to various factors such as temperature drift and load, this calibration may need additional attention in order for the output voltage to respond as expected to voltage adjustments. This is where the offset command comes in. Voltage offset (positive or negative) can be added to the output voltage set point to help a UFE produce more accurate output voltages. In order to use this command, the signed 7-bit, 2's complement, offset control code, Voffcc, must be calculated by using the following formula:

48 V unit: $V_{offset} = (V_{offcc}*0.977)/63$

24 V unit: $V_{offset} = (V_{offcc}*0.49)/63$

Where Voffset represents the actual voltage adjustment (positive or negative from current output voltage level) that will be implemented when the decimal value control code, Voffcc (-64 to 63), is entered into the command. For the 48 V UFEPS the resolution is still about 15.5 mV per step, with a maximum swing of 0.977V in either the positive or negative direction. For the 24V UFEPS the resolution is still about 7.8 mV per step, with a maximum swing of 0.49V in either the positive or negative direction.

Care should be taken to keep the output voltage plus offset voltage within the specified output range of the UFE of 42 V to 57 V or 21 V to 28.5 V, as adjustment outside of this range is not possible.

Within command #2, there is a Control bit Status Byte (CbSB) containing six control bits. These bits can change the general power conversion parameters as well as run certain functionality tests or change the default power up operation of the UFE. See details in Table 3 ("DF" denotes the default setting for the control bit).

The Inhibit control bit (Inhcb) can enable or disable power conversion in the UFE. It can also be used to reset the UFE after a latching O V condition. This bit does not affect the 11 V auxiliary voltage.
The Output Voltage Droop control bit (Vdrpcb) can enable or disable droop on the output voltage. Voltage droop is used to force paralleled UFEs to share current without the use of the discrete "Ishare" pin.

The Output Voltage active current sharing control bit (Ishrcb) can enable or disable active current sharing. Active current sharing can be used in place of output voltage droop. The benefit of using active current sharing is that the output voltage does not change with load and the level will correspond directly and accurately to the three output voltage change commands. The disadvantage of using active current sharing is the requirement of the use of the Ishare pin between separate UFEs. Please note that if both Vdrpcb and Ishrcb are cleared only droop control will be used.

The I²C communications watchdog timer control bit (WDcb) can enable or disable the 45-second I²C communications watchdog timer. If enabled, I²C traffic specific to each UFE is expected at least once every 45 seconds. If a UFE does not receive an I²C message in this 45 seconds, it will revert to factory default settings.

The out voltage or-ing FET test control bit (ORtcb) can be used to verify the functionality of the output or-ing FETs. In order to test the or-ing FET's, this bit must be set. Note that this test should only be performed one unit at a time in a redundant system that will not be affected by one unit being removed from the system for 1 second. The results from this test are available in an alarm status byte 1.5 seconds after the test is initiated. This bit will be cleared automatically when the test is complete.

The default Memory control bit (Memcb) can be used to change the default operation of a UFE. When the Memcb is set, a UFE will save the control byte, output voltage setting and output voltage offset in EEPROM. This can be useful to change the default power up state if desired. Please note that as long as this Memcb is set, every time the control byte, output voltage setting or output voltage offset is changed, the value is stored into non-volatile memory. The maximum write capability of this memory is 1,000,000 erase/write cycles. Care should be taken not to exceed this 1,000,000-erase/write-cycle limit. For example, if a lot of changes were going to be made to the output voltage or control byte, rapidly and for a long duration, it would be best not to set this bit. However, if few changes will be made over time, then this bit can be useful to change the default operation of the supply, or force the supply to retain settings for restoration after a power interruption.

Inhcb	DESCRIPTION
0 (DF)	Inhibit bit is inactive, output power conversion is active and enabled
1	Inhibit bit is active, output power conversion is inactive and disabled

WDcb	DESCRIPTION
0	I²C Watchdog inhibit is inactive, I²C Watchdog timer is enabled
1 (DF)	I²C Watchdog inhibit is active, I²C Watchdog timer is disabled

Vdrpcb	DESCRIPTION
0 (DF-48 V)	Voltage Droop Inhibit bit is inactive, output voltage has droop
1 (DF-24 V)	Voltage Droop Inhibit bit is active, output voltage has no droop

ORtcb	DESCRIPTION
0 (DF)	Or-ing FET test bit is inactive, Or-ing FEET test is active
1	Or-ing FET test bit is inactive, Or-ing FEET test is inactive

Ishrcb	DESCRIPTION
0 (DF-24 V)	Active Current Sharing Inhibit bit is inactive, Active Current Sharing is enabled
1 (DF-48 V)	Active Current Sharing Inhibit bit is active, Active Current Sharing is disabled

Memcb	DESCRIPTION
0 (DF)	Unit will power up with all factory defaults
1	Unit will power up in the same state as it was at power down

Table 3 - Control Bit Functionality

In order to prevent an accidental inhibit of a UFE over I²C, an activation key must be used to unlock the control bits feature. In order to toggle any of the control bits, the correct activation key byte of 0xA6 must be sent in the preceding byte. If the key is not correct, none of the control bits will be able to change states. The activation key must be sent each time any control bit is to be changed. Command #2 is constructed of four bytes, illustrated in Table 4.

	I²C ADDRESS BYTE	COMMAND # BYTE	ACTIVATION KEY	CONROL BITS	7-BIT V_{offcc}
BYTE	5 (MSB)	4	3	2	1 (LSB)
Bit	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Content	UFE Address 0	0 0 0 0 0 0 1 0	1 0 1 0 0 1 1 0	X X Memcb Ortcb WDcb Ishrcb Vdrpcb Inhcb	X Voffcc (-64 to 63) - 7-bit 2's comp

X - Denotes Not Used or Don't Caare Bit

Table 4 - Individual Offset and Control Command Structure

Each UFE is capable of storing up to 256 bytes of information in EEPROM, without the additional, optional 256 bytes of external EEPROM. This space is shared between user data, Artesyn manufacturing data, and certain microprocessor variables that need to be kept in non-volatile memory for variable restoration at startup. User data will be stored from location 0 to 174 (175 bytes total). To allow small portions of data to be written to and changed at a time, an offset byte is used. Data is written from the offset byte until the MSB of the data, which is the LSB of the I²C communication, or the master terminates the communication with a stop condition.

The fourth write command is the UFE Information Storage Command (command #4). It is constructed of multiple bytes, determined by the I²C master, illustrated in Table 5.

	I²C ADDRESS BYTE	COMMAND # BYTE	DATA OFFSET	START OF DATA	END OF DATA
BYTE	N (MSB)	N - 1	N - 2	N - 3	1 (LSB)
Bit	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Content	UFE Address	0 0 0 0 0 1 0 0	Data Offset (0-174)	Data at Offset	174th byte of Data

Table 5 - UFE Information Storage Command Structure

In order to simplify operation, only one kind of I²C read is available. The memory mapping locations are placed specifically to provide the most valuable and urgent information early on in the read and less urgent information later in the message. It is acceptable to read out anywhere from 1 byte up. The entire read message consists of 247 bytes. After the 247th byte the information simply repeats, starting with byte 1 again. The memory map is illustrated in Table 6.

BYTE	248 (MSB)								247 through 246	245							244								243							
Bit	7	6	5	4	3	2	1	0	15.....0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Content	UFE Address							1	ASW	Iout								Vout								Pout							

BYTE	242	241	240	239 through 237	236 through 207
Content	TUFE	Tamb	CbSB	POT	APNR

BYTE	206 through 197	196 through 187	186 through 184	183 through 176
Content	ASN	AMN	AMDT	Reserved

BYTE	175 through 1 (LSB)
Content	General Information Storage, Address 0 -174

Table 6 - Address Locations for a Complete I²C Read Command

The Alarm Status Word (ASW) is used to quickly relay important information about the UFE. The byte is detailed in Table 7.

BYTE	2 (MSB)								1 (LSB)							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Content	X	EEFault	AmbOTWrn	UFEOTWrn	PSen	V12Err	EEBusy	FanErr	AmbOT	UFEOT	OutOR	OutCL	OutOV	OutUV	LineOv	LineUV

Table 7 - Alarm Status Word Sturcture

Where:

Line UV = Input Line Under Voltage. If set, indicates that the AC line is too low for Operation, below 176 Vac rms. This alarm will clear automatically when the Input line is in acceptable range.

LineOV = Input Line Over Voltage. If set, indicates that the AC line is too high for Operation, above 285 Vac rms ±3%. This alarm will clear automatically when the Input line is in acceptable range.

OutUV = DC output Under Voltage. If set, indicates that the DC output has experienced an under voltage condition. This alarm will clear automatically when the output is of sufficient level again.

OutOV = DC output Over Voltage. If set, indicates that the DC output has experienced an over voltage condition. This alarm can be reset by toggling the Inhcb or PS-EN-L discrete pin.

OutCL = DC output Current Limit. If set, indicates that the DC output is in current limit. This alarm will clear automatically when the condition causing the current limit is removed from the UFE output.

OutOR = DC output OR-ing. If set, indicates that the or-ing function of the output has a problem and is not functioning. Only valid 1.5 seconds after the test is initiated by setting the Ortcb in write command #2. This alarm can be reset by toggling the Inhcb or PS-EN-L discrete pin.

UFEOT = UFE Overtemperature. If set, indicates that the internal temperature of the UFE is too high for operation and the unit will be shutting down or is shut down already. This alarm will clear automatically when the internal temperature is in acceptable range again.

AmbOT = Ambient Overtemperature. If set, indicates that the internal ambient temperature is too high for operation and the unit will be shutting down or is shut down already. This alarm will clear automatically when the ambient temperature is in acceptable range again.

FanErr = Fan Error. If set, indicates that the fan converter is not functioning properly and is putting out too high or too low of a voltage than is acceptable for a given operation set point. This alarm will clear automatically when the fan converter output is at an acceptable level again.

EEBusy = EEPROM is busy. If set, indicates that the EEPROM is in the process of writing information. While this bit is set, it is not possible to read out or write in anything from general information storage. This prevents data errors caused by interruptions when data is being

written to EEPROM. It takes up to 8ms to completely write 1 byte of EEPROM. This alarm will clear automatically when the EEPROM write is finished.

V12Err = +12Vaux Error. If set, indicates that the +12V aux is not functioning properly and is putting out under 10 V or over 14 V. This alarm will clear automatically when the +12V aux output is at an acceptable level again.

PSen = Power supply Enable. If set, UFE power conversion is not active due to the discrete PS-EN-L pin being high. This alarm will clear automatically when the discrete PS-EN-L pin is low.

UFEOTWrn = UFE overtemperature warning. If set, the internal tem perature of the UFE is approaching the overtemperature fault shutdown temperature. This alarm will clear automatically when the internal temperature is in acceptable range again.

AmbOTWrn = Ambient overtemperature warning. If set, the ambient temperature of The UFE is approaching the overtem perature fault shutdown temperature. This alarm will clear automatically when the ambient temperature is in acceptable range again.

EEFault = EEPROM checksum fault. If set, the checksum for the internal EEPROM didn't validate at power up. This checksum is calculated and stored each time the input voltage is removed, and is validated at power up. This alarm can be reset by toggling the Inhcb or PS-EN-L discrete pin.

The output current reading byte (Iout) can be used to indicate what the approximate output current level (Io, in Amps) is from a given UFE in a system. Encoding for this byte is from the following equation:

$$Io = (Iout \bullet Ilim) / 200$$

Where Ilim is the decimal value, 8-bit, of the output current limit's minimum specified value. A value of Iout = 0 represents 0A output (ideally), and a value of Iout = 200 represents current limit at the output of the UFE. A value of 220 will indicate 10% over minimum current limit. This yields a resolution of 0.5% of current limit per bit. For example, a 48V UFEPS has a minimum current limit of 47.8A (52A – 8% = 47.8 A) at the 2000 W power level. If Iout reports 100, then the output current is 23.9A. The accuracy of the Iout byte is +/- 15%. This accuracy is only valid from above 20% of Ilim to Ilim, due to circuit limitations.

The Output Voltage reading byte (Vout) can be used to indicate what the approximate output voltage level (Vo, in Volts) is from a given UFE in a system. Encoding for this byte is from the following equation:

$$Vo = (Vout / 4)$$

Where Vout is an 8-bit representation of the output voltage. The resolution of this signal is therefore 0.25V/bit. The accuracy of the Vout byte is +/-5% and the minimum value reported is about 17, or 5.75V, due to circuit limitations.

The rated output power byte (Pout) can be used to indicate what the output power rating is for a given UFE in a system. This byte is not an indication of actual output power being delivered. The byte is encoded according to the following equation:

$$RatedPower = Pout \bullet 10$$

Where Pout is the decimal value (0-255) of the rated output power and RatedPower is the calculated rated output power in Watts. The resolution is 10Watts per bit with a maximum representation of 2550Watts. For example, for a 2000 Watt UFE, Pout would equal 200.

The internal temperature indication byte, TUFE can be used to indicate what the internal temperature is of a UFE. Scaling is 1°C/bit, two's complement, to represent negative numbers. Temperatures from –41°C to 126°C can be reported.

The ambient temperature indication byte, Tamb can be used to indicate what the ambient temperature is of a UFE. Scaling is 1°C/bit, two's complement, to represent negative numbers. Temperatures from –41°C to 126°C can be reported.

The CbSB is used to indicate the current settings of the control bits.

The UFE provides a running total of the number of hours a UFE has been in operation, in the form of a 3-byte number, the Power On Time (POT), detailed in Table 8.

BYTE	3 (MSB)								2								1 (LSB)							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Content	High POT Byte								Middle POT Byte								Low POT Byte							

Table 8 - Power On time (POT) Bytes Structure

The resolution of these bytes is 1 hour per bit, with a maximum representation of 114 years of operation (up to 1,000,000 erase/write cycles on EEPROM max). This is because it takes at least 17 bits to represent 10 years of operation with 1 hour per bit resolution. The internal counter increments as long as the AC line voltage is present and valid. The accuracy of this timer is ±1%, or ±36 seconds out of every hour.

The UFE stores certain information related to it's manufacturing. This information consists of 61 bytes of information stored and protected in EEPROM addresses 175 through 235. This information is ASCII encoded and all fields are filled with trailing ASCII space (20h) characters in order to fill the entire allowed space.

The Artesyn Part Number and Revision (APNR) field consists of 30 bytes in the form: "UFEXXXX-XXXXXXXXXXXXXXXXXXXXXX", where X represents variable data. An example for the standard 2000 W 48 V unit would be: "UFE2000-96S48CJ Rev 1P ". Note the trailing ASCII spaces (20h) required to fill the entire 30 bytes of available space.

The Artesyn Serial Number (ASN) field consists of 10 bytes in the form "XXXXXXXXXX", where X represents variable data.

The Artesyn Manufacturer Name (AMN) field consists of 10 bytes, “ATSN ”.

The Artesyn Manufacture Date and Time (AMDT) field consists of 3 bytes. The time is calculated in the number of minutes elapsed from start time 12:00 AM, January 1st 1996. This gives the capability of representing date and time up to the year 2026, with 1-minute resolution. This data takes the form of LSB - MSB.

The reserved field of 8 bytes is reserved for future use and will consist of 8 spaces for now.

3. I²C Serial Bus Requirements

Data rates of up to 400 kHz are supported. To ensure reliable and compliant I²C communications, a maximum rise time of 300 ns on both the SDA and SCL lines must be achieved. The maximum acceptable fall time is 300 ns on these lines. Rise and fall time is defined between 0.3 VDD and 0.7 VDD. For a VDD of +5 V, the rise and fall time would therefore be defined between 1.5 V and 3.5 V. Each UFE also adds about 130 pF to an I²C bus, so it is recommended that no more than 3 UFEs be connected to any I²C bus at a time without the use of an I²C buffer. This capacitance is due to the FET isolation/hot plug circuit, ESD protection device, as well as parasitic capacitance due to shielded routing considerations. See Figures 1 and 2 for details.

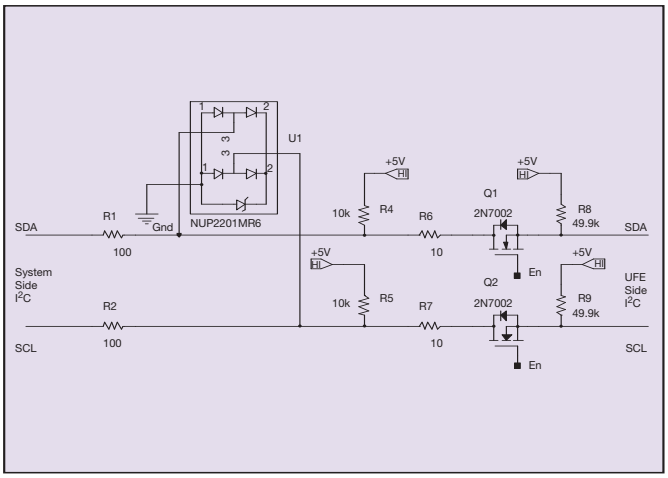

Figure 1 - Basic I²C Schematic

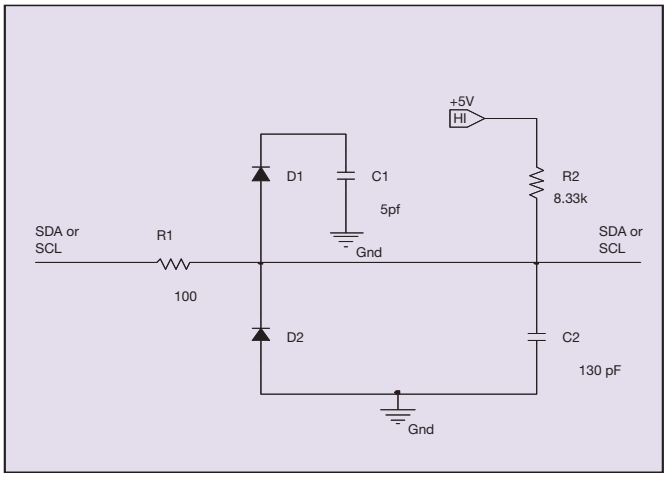

Figure 2 - Equivalent Circuit Model for the Basic I²C Schematic

There is a maximum I²C message dead time timer that can't be disabled. The I²C interface will time out and hardware reset if there is more than 20ms between bytes or bits within a message. This is done to prevent problems that might occur when any devices are hot-plugged onto the I²C lines, or for any other reason. So if a device happens to "lock" the I²C bus upon hot-plug, this timer will timeout, the UFE will disregard the rest of the I²C message and reset its I²C hardware.

The I²C data structure used by the UFEs fully conform to the 7 bit addressing protocol of the Philips I²C bus specification. The UFEs act as slaves on the I²C bus and follow the I²C bus format of most significant byte first, most significant bit first, as illustrated in Table 9.

Transfer from master - I²C Write

	BYTE N ADDRESS BYTE									BYTE N-1 COMMAND BYTE									BYTE 2 DATA									BYTE1 DATA									
Bit	S	7	6	5	4	3	2	1	0	A	7	6	5	4	3	2	1	0	A	7	6	5	4	3	2	1	0	A	7	6	5	4	3	2	1	0	A	P

Transfer to master - I²C Read

	BYTE N ADDRESS BYTE									BYTE N-1 COMMAND BYTE									BYTE 2 DATA									BYTE1 DATA									
Bit	S	7	6	5	4	3	2	1	0	A	7	6	5	4	3	2	1	0	A	7	6	5	4	3	2	1	0	A	7	6	5	4	3	2	1	0	A	P

From Master to Slave

From Slave to Master

A = Acknowledge bit
S = Start Condition
P = Stop Condition

Table 9 - I²C Bus Data Structure

Each UFE determines it's own unique address by use of the discrete pins, PS-ID0 through PS-ID3. This allows for up to 16 unique addresses to be included in a system. However, when the optional EEPROM extended memory is installed, only 8 unique addresses can be obtained in a system because of addressing limitations in the EEPROM module only using discrete pins PS-ID0 through PS-ID2. The optional EEPROM extended memory module is Atmel part number AT24C02 or ST Microelectronics part number M24C02. This extended memory module is addressed separately from the UFE microprocessor on the I²C bus and can be used any time the UFE is inserted into a system and is fully functional. Optional EEPROM is offered so that the user can either use the available 175 bytes of internal EEPROM, or add an additional 256 bytes if desired.

The UFE I²C addressing for the microprocessor and optional EEPROM extended memory module is detailed in Table 10.

BYTE	BIT VALUE					COMMENTS
	Micro I2C Read	Micro I²C Write	All V-adjust Command	OPTIONAL EEPROM I²C Read	OPTIONAL EEPROM I²C Write	
7	1	1	0	1	1	MSB
6	1	1	0	0	0	
5	1	1	0	1	1	
4	PS-ID3	PS-ID3	0	0	0	
3	PS-ID2	PS-ID2	0	PS-ID2 = A2	PS-ID2 = A2	
2	PS-ID1	PS-ID1	0	PS-ID1 = A1	PS-ID1 = A1	
1	PS-ID0	PS-ID0	0	PS-ID0 = A0	PS-ID0 = A0	
0	1	0	0	1	0	LSB, I²C Read = "1", I²C Write = "0"

Table 10 - I²C Addressing Details

UFEPS NUMBER	PS-ID3	PSID2	PSID1	PSID0	MICRO I²C ADDRESS	*EEROM I²C ADDRESS
1	0	0	0	0	E0	A0
2	0	0	0	1	E2	A2
3	0	0	1	0	E4	A4
4	0	0	1	1	E6	A6
5	0	1	0	0	E8	A8
6	0	1	0	1	EA	AA
7	0	1	1	0	EC	AC
8	0	1	1	1	EE	AE
9	1	0	0	0	F0	A0
10	1	0	0	1	F2	A2
11	1	0	1	0	F4	A4
12	1	0	1	1	F6	A6
13	1	1	0	0	F8	A8
14	1	1	0	1	FA	AA
15	1	1	1	0	FC	AC
16	1	1	1	1	FE	AE

***EEPROM is optional**

Table 11 - UFE Numbering Reference

So in this setup, I2C addresses from E0h to FEh are valid for the microprocessor, and addresses from A0h to AEh are valid for the optional EEPROM. Because these addresses are determined within the UFE's microprocessor firmware, the range of these addresses is capable of modification at the user's request, by application.

If the user will be using the Artesyn designed chassis, PS-ID2 and PS-ID3 are set up with two DIP switches on the chassis, and PS-ID0 and PS-ID1 are setup within the chassis. This allows for minimal user setup, however it does limit the system to incorporate only four chassis each with only three power supplies, for a total of twelve unique addresses. The UFE numbers of **4**, **8**, **12**, and **16** are not valid in this type of setup. In addition, if the optional EEPROM is being used, only six unique addresses are available for the EEPROM, making it mandatory to have multiple I^2C busses with more than six units in a system.

If more than sixteen UFEs are desired for a system, it is always possible to isolate the I^2C bus, with a buffer/driver enable line, to a chassis so that the same I^2C address can be used multiple times. This type of setup alleviates both the I^2C bus capacitance limitation as well as the maximum number of UFEs that can be incorporated into a system.